**A Highly Efficient and Reliable Inverter Configuration Based Cascaded Multilevel Inverter for PV Systems**

**Abstract**

This paper presents an improved cascaded multilevel inverter (CMLI) based on a highly efficient and reliable configuration for the minimization of the leakage current. Apart from a reduced switch count, the proposed scheme has additional features of low switching and conduction losses. The proposed topology with the given pulse width modulation (PWM) technique reduces the high frequency voltage transitions in the terminal and common mode voltages. Avoiding high-frequency voltage transitions achieves the minimization of the leakage current and reduction in the size of electromagnetic interference filters. Furthermore, the extension of the proposed CMLI along with the PWM technique for 2m + 1 levels is also presented, where m represents the number of photovoltaic (PV) sources. The proposed PWM technique requires only a single carrier wave for all 2m + 1 levels of operation. The total harmonic distortion of the grid current for the proposed CMLI meets the requirements of IEEE A comparison of the proposed CMLI with the existing PV multilevel inverter topologies is also presented in the paper. Complete details of the analysis of PV terminal and common-mode voltages of the proposed CMLI using switching function concept, simulations, and experimental results are presented in the paper.

Introduction

Transformerless multilevel inverter (MLI) topologies are gaining importance due to their advantages such as high efficiency, low switch count, low weight, and reduced size. However, removal of the transformer eliminates the galvanic isolation between the photovoltaic (PV) array and the output load. Removal of galvanic isolation increases the leakage current compromising the safety in PV systems. It has led to the development of various safety standards for the PV systems, which restrict the value or magnitude of leakage current flow in the PV system. Apart from leakage current minimization, there is a continuously increasing demand for high-quality Manuscript received. This requirement has led to the use of MLI in the transformerless PV systems. In the literature, many topologies or configurations of MLIs are proposed for the minimization of leakage current for their application in the transformerless PV systems. These configurations employ two methods for minimization of the leakage current. One method is based on maintaining the common-mode voltage (CMV) constant, while the other method is based on the minimization of the high-frequency transitions in the terminal and CMVs. The given MLI configuration consists of eight switches for the generation of three levels in the output voltage. This topology reduces the switching losses but has the drawback of high conduction losses during both turn ON and zero voltage states. The given MLI configuration has an asymmetric operation during each half-cycle of the fundamental component of the grid voltage. The inherent asymmetry in each half-cycle causes a dc offset in the MLI output voltage. Furthermore, the requirement of an additional number of switches for more than three-level operation limits its application.i have proposed another interesting transformerless PV MLI topology to reduce the leakage current by maintaining CMV constant. This MLI topology uses six switches for the generation of three levels in the inverter output voltage. This circuit configuration results in high switching and conduction losses. Furthermore, this MLI topology cannot be extended to more than three levels in the output voltage. I have proposed another efficient three-level MLI for the minimization of leakage current by maintaining CMV constant. The given topology low conduction and switching losses. However, this configuration suffers from the disadvantage of a high number of device count. This MLI topology consists of six switches and two diodes. Apart from resulting in high conduction losses, this topology is less amenable for an extension to a higher number of levels in the output voltage. Another important method to minimize the leakage current is by the elimination of high-frequency voltage transitions in the CMV.

**Salient features of the proposed cascaded MLI (CMLI) are as follows**

1) The topology uses eight switches for the generation of five levels in the output voltage.

2) During the zero voltage state only one switch and one diode conduct.

3) In the proposed topology, four switches are operated at a low switching frequency, which reduces the switching losses.

4) The dead band in the PWM technique does not affect the CMV.

5) The proposed inverter can be easily cascaded to achieve more than five levels in the output. Rest of the paper is organized into eight sections.

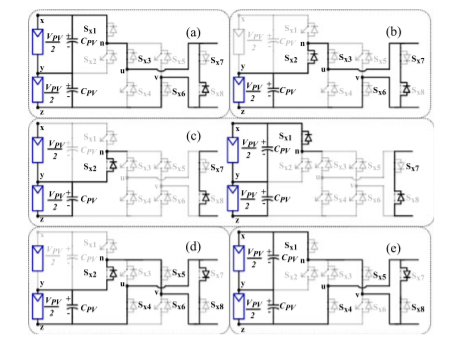
the working principle and the operation for the proposed five-level grid-connected CMLI along with the generalized structure. The details of the PWM technique employed with its generalization for 2m + 1 levels are explained in Section III. Section IV gives the details of the maximum power point tracking (MPPT) algorithm which can be applied to the proposed five-level CMLI. This is followed by the analysis of terminal and CMVs for the proposed CMLI the simulation results of the proposed five-level grid connected CMLI. Section VII shows the experimental results of the proposed five-level and nine-level CMLI. Comparison of the proposed CMLI with the other existing PV MLI topologies in the literature is presented.

. 1. Proposed five-level grid-connected CMLI with PV and parasitic elements

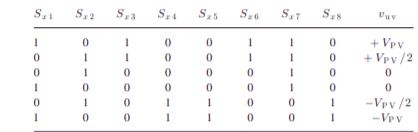
II. OPERATION OF THE PROPOSED CASCADED FIVE-LEVEL MLI.

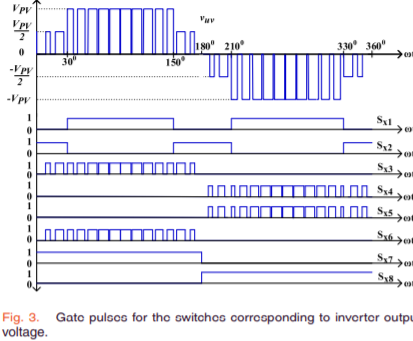
The schematic circuit diagram of the proposed five-level CMLI for the PV system. The given configuration consists of two converters (Conv-1 and Conv-2). Conv-1 is a half-bridge inverter comprising two switches Sx1 and Sx2 . The Conv-2 comprises of a highly efficient and reliable inverter configuration with six switches (Sx3 –Sx8 ). Among the six switches, four switches (Sx3 –Sx6 ) in Conv-2 constitute an H-bridge circuit. The remaining two switches Sx 7 and Sx8 in Conv-2 are bidirectional switches. The switches in the Conv1 are used to generate the voltage levels of VPV and VPV /2. When switch Sx1 is turned ON, the voltage VPV is applied at the terminal n with respect to the terminal z. Similarly, the terminal n attains the voltage VPV /2 when switch Sx2 is turned ON. The switches Sx1 and Sx2 are complementary in nature. The generated voltage levels at the terminal n of Conv-1 are given as an input to the Conv-2. The Conv-2 generates the positive, negative, and zero levels of corresponding input voltage (voltage between the terminals n and z) across the load. The bidirectional switches Sx7 and Sx8 provide the free-wheeling path during zero voltage state. The output of the five-level CMLI is connected to the grid through an LCL filter. It consists of inverter side inductance Li, capacitance, and grid side inductance Lac . The resistance Rd in the shunt branch of the filter is used as a damping resistor. The resistance refers to the grid side resistance, and the resistance indicates resistance in the ground path. The variable vac refers to instantaneous grid voltage. The variables Rp and Cp refer to the parasitic resistance and capacitance in the PV system, respectively, shown with dotted lines. The parasitic capacitance in the PV system forms a resonant circuit with the filter inductances. The variables io , ic , and iac denote the output current of the five-level CMLI, current flowing through shunt branch of the filter, and the current flowing into the grid, respectively. The current leak indicates the leakage current flowing from the PV array into the ground through parasitic capacitance.

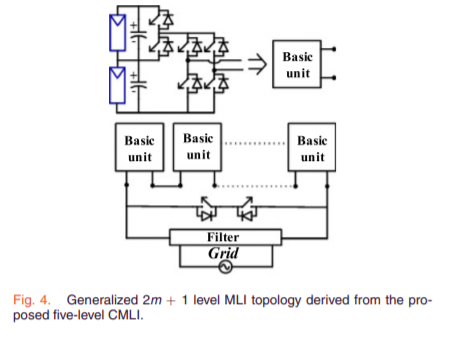
**Circuit diagram**

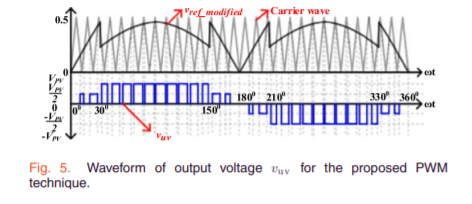


**switching operation**









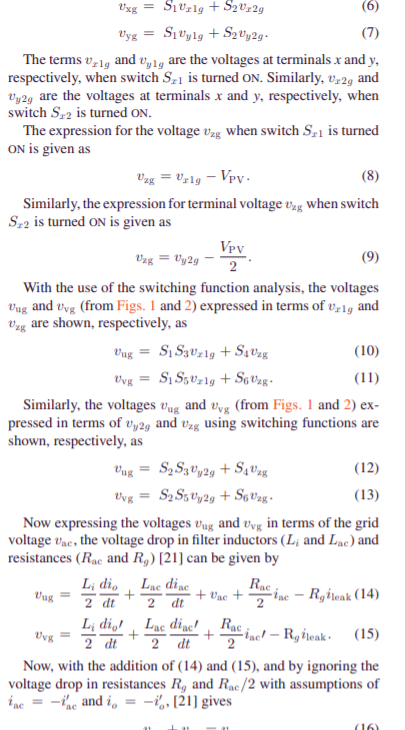
**INTEGRATION OF MPPT FOR THE PROPOSED FIVE-LEVEL CMLI INTEGRATION OF MPPT FOR THE PROPOSED FIVE-LEVEL CMLI**

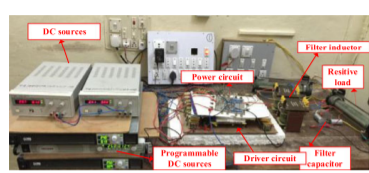
The well-known perturb and observe algorithm [20] is employed for the two PV sources (considering five-level operation) individually to track maximum power point (MPP). Thus, each MPPT algorithm tracks the MPP for respective PV sources. To track the MPP, the required information of

1) the average values of the two PV source voltages (VPV1 and VPV2 for the PV sources PV1 and PV2 , respectively).

2) the currents (IPV1 and IPV2 for the PV sources PV1 and PV2 , respectively) are sensed and then given to their respective MPPT algorithms. The MPPT algorithms then use the sensed values of the PV voltages and currents for the calculation of the individual values of the modulation indices ma1 and ma2 for the two PV sources PV1 and PV2 , respectively. The output two MPPT algorithms are then utilized for the calculation of overall modulation index.

**ANALYTICAL EXPRESSIONS OF PV TERMINAL VOLTAGE AND COMMON-MODE VOLTAGE FOR THE PROPOSED CASCADED FIVE-LEVEL INVERTER.**





Basic block diagram of five level inverter

A—Asymmetry operation during positive and negative cycle of the MLI. B—Number of devices conducting in zero voltage state including switches and diodes.

C—Number of devices used in the MLI. s—Number of switches used in the MLI.

d—Number of diodes used in the MLI. D—Number of devices including switches and diodes conducting. p—During the positive half-cycle of the grid voltage. n—During the negative half-cycle of the grid voltage

. E—Number of switches operating at high switching frequency. F—Number of switches operating at low switching frequency.

**DC to DC converter**

In electronics engineering, a DC to DC converter is a circuit which converts a source of

direct current from one voltage to another. It is a class of power converter.

DC to DC converters are important in portable electronic devices such as cellular phones

and laptop computers, which are supplied with power from batteries. Such electronic devices

often contain several sub-circuits with each sub-circuit requiring a unique voltage level different

than that supplied by the battery (sometimes higher or lower than the battery voltage, and

possibly even negative voltage). Additionally, the battery voltage declines as its stored power is

drained. DC to DC converters offer a method of generating multiple controlled voltages from a

single variable battery voltage, thereby saving space instead of using multiple batteries to supply

different parts of the device.

**Conversion methods**

Linear A simple method of converting one voltage to another is a circuit known as a voltage

divider. This technique uses resistors in series with the voltage supply to provide a lower voltage. However, this method suffers serious drawbacks:

 Provides no voltage regulation

 Requires knowledge of the resistance of the load

 Poor efficiency, which also leads to excess heat dissipation

 Impossible to generate voltages higher than the supply voltage

 Impossible to generate negative voltages, unless the system ground is defined by a node

in the resistor network.

Any kind of voltage regulator solves the first two problems, however, linear regulators.

**Switched-mode conversion**

Between the input and the output, generally allowing differences in the

input-output ground Electronic switch-mode DC to DC converters are available to convert one DC voltage

level to another. These circuits, very similar to a switched-mode power supply, generally

perform the conversion by applying a DC voltage across an inductor or transformer period

of time (usually in the 100 kHz to 5 MHz range) which causes current to flow through it and

store energy magnetically, then switching this voltage off and causing the stored energy to be

transferred to the voltage output in a controlled manner. By adjusting the ratio time the

output voltage can be regulated even as the current demand changes. This conversion method is more power efficient (often 80% to 95%) than linear voltage conversion which dissipate

unwanted power. This efficiency is beneficial to increasing the running time of battery

Isolated DC-DC converters convert a DC input power source to a DC output power while

maintaining isolation potentials in the range of hundreds or thousands of volts. They can be an

exception to the definition of DC-DC converters in that their output voltage is often (but not

A current-output DC-DC converter accepts a DC power input, and produces as its output

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topologies of the DC to DC converter can generate voltages higher, lower, higher and lower or negative of the input voltage; their names are:

 Buck

 Boost

 Buck-boost

 Ćuk

In general, the term &quot;DC to DC converter&quot; almost always refers to one of these switchingconverters.

Switching DC to DC converters are available in a wide variety of input and fixed or output voltages.

DC to DC converters are now available as integrated circuits needing minimal extra

components to build a complete converter. DC to DC converters are also available as complete

hybrid circuits, ready for use within an electronic device.

**DC-DC CONVERTER BASICS**

A DC-to-DC converter is a device that accepts a DC input voltage and produces a DC

output voltage. Typically the output produced is at a different voltage level than the input. In

addition, DC-to-DC converters are used to provide noise isolation, power bus regulation, etc.

This is a summary of some of the popular DC-to-DC converter topolopgies:

**BUCK CONVERTER STEP-DOWN CONVERTER**

In this circuit the transistor turning ON will put voltage Vin on one end of the inductor.

This voltage will tend to cause the inductor current to rise. When the transistor is OFF, the

current will continue flowing through the inductor but now flowing through the diode. We

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Isolated DC-DC converters convert a DC input power source to a DC output power while maintaining isolation between the input and the output, generally allowing differences in the input-output ground potentials in the range of hundreds or thousands of volts. They can be an exception to the definition of DC-DC converters in that their output voltage is often (but not always) the same as the input voltage.

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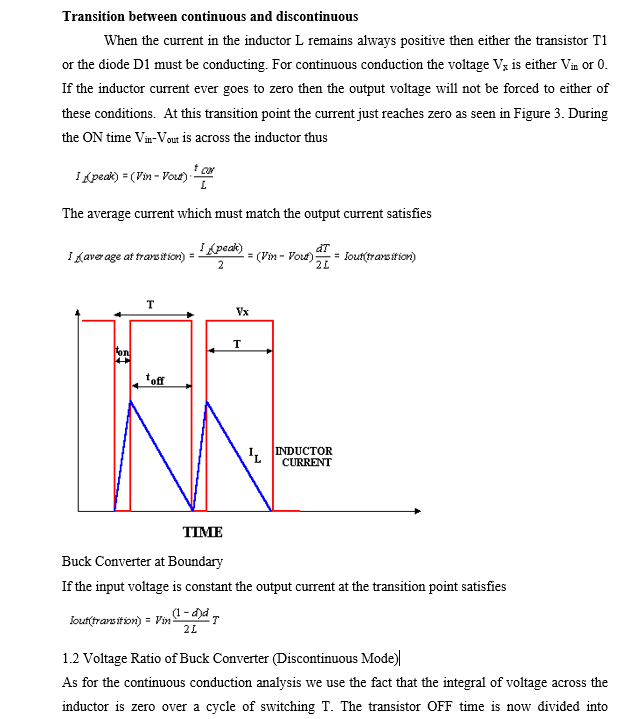
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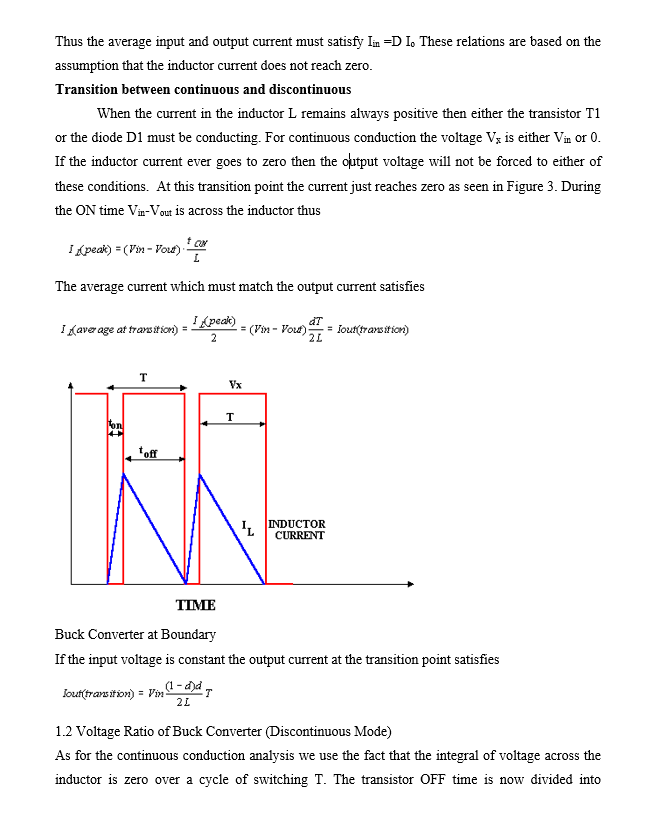
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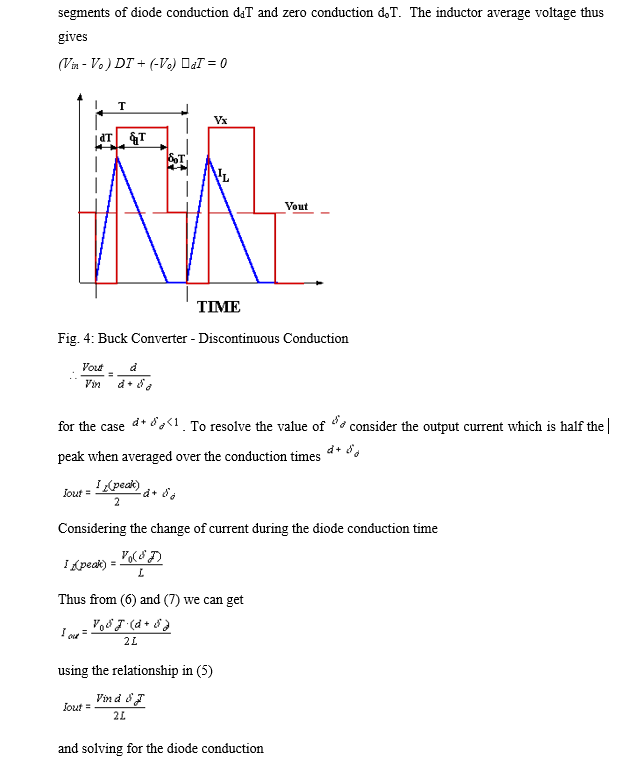
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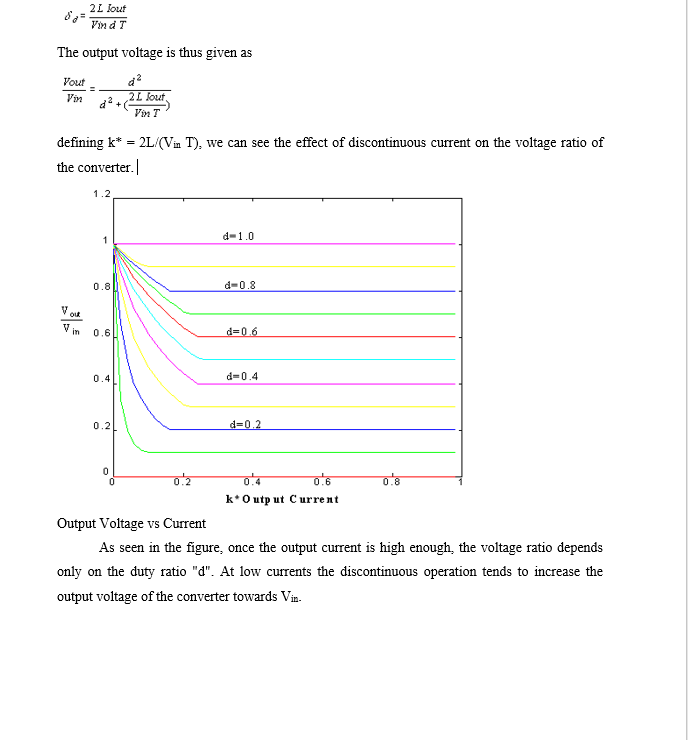
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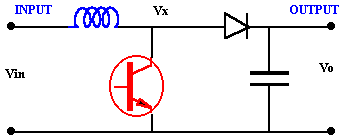








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**Boost converter**

While the transistor is ON Vx =Vin, and the OFF state the inductor current flows through the diode giving Vx =Vo. For this analysis it is assumed that the inductor current always remains flowing (continuous conduction). The voltage across the inductor and the average must be zero for the average current to remain in steady state

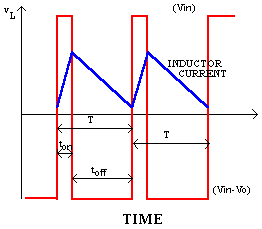
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This can be rearranged as

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and for a lossless circuit the power balance ensures

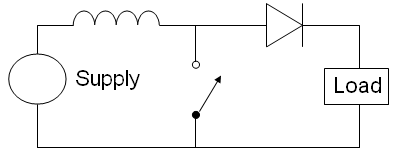
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Voltage and current waveforms (Boost Converter)

# **Since the duty ratio "D" is between 0 and 1 the output voltage must always be higher than the input voltage in magnitude. The negative sign indicates a reversal of sense of the output voltage.**

A **boost converter** (**step-up converter**) is a [power converter](http://en.wikipedia.org/wiki/Power_converter) with an output DC voltage greater than its input DC voltage. It is a class of [switching-mode power supply (SMPS)](http://en.wikipedia.org/wiki/Switched-mode_power_supply) containing at least two [semiconductor](http://en.wikipedia.org/wiki/Semiconductor) switches (a [diode](http://en.wikipedia.org/wiki/Diode) and a [transistor](http://en.wikipedia.org/wiki/Transistor)) and at least one [energy](http://en.wikipedia.org/wiki/Energy) storage element. Filters made of [capacitors](http://en.wikipedia.org/wiki/Capacitor) (sometimes in combination with [inductors](http://en.wikipedia.org/wiki/Inductor)) are normally added to the output of the converter to reduce output voltage ripple.



## Overview

Power can also come from DC sources such as batteries, solar panels, rectifiers and DC generators. A process that changes one DC voltage to a different DC voltage is called DC to DC conversion. A boost converter is a [DC to DC converter](http://en.wikipedia.org/wiki/DC_to_DC_converter) with an output voltage greater than the source voltage. A boost converter is sometimes called a step-up converter since it “steps up” the source voltage. Since power (P = VI) [must be conserved](http://en.wikipedia.org/wiki/Law_of_conservation_of_energy), the output current is lower than the source current.

A boost converter may also be referred to as a '[Joule thief](http://en.wikipedia.org/wiki/Joule_thief)'. This term is usually used only with very low power battery applications, and is aimed at the ability of a boost converter to 'steal' the remaining energy in a battery. This energy would otherwise be wasted since a normal load wouldn't be able to handle the battery's low voltage.

## History

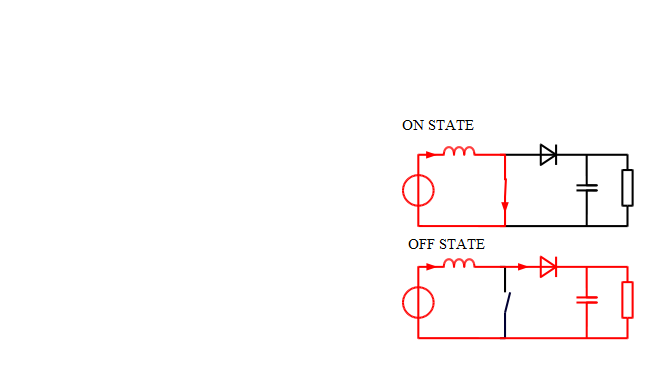
For high efficiency, the [SMPS](http://en.wikipedia.org/wiki/Switched-mode_power_supply) switch must turn on and off quickly and have low losses. The advent of a commercial [semiconductor](http://en.wikipedia.org/wiki/Semiconductor) switch in the 1950’s represented a major milestone that made SMPSs such as the boost converter possible. Semiconductor switches turned on and off more quickly and lasted longer than other switches such as [vacuum tubes](http://en.wikipedia.org/wiki/Vacuum_tube) and electromechanical relays. The major [DC to DC converters](http://en.wikipedia.org/wiki/DC_to_DC_converter) were developed in the early 1960s when semiconductor switches had become available. The [aerospace](http://en.wikipedia.org/wiki/Aerospace) industry’s need for small, lightweight, and efficient power converters led to the converter’s rapid development.

Switched systems such as SMPS are a challenge to design since its model depends on whether a switch is opened or closed. R.D. Middlebrook from [Caltech](http://en.wikipedia.org/wiki/Caltech) in 1977 published the models for DC to DC converters used today. Middlebrook averaged the circuit configurations for each switch state in a technique called state-space averaging. This simplification reduced two systems into one. The new model led to insightful design equations which helped SMPS growth.

## Applications

Battery powered systems often stack cells in series to achieve higher voltage. However, sufficient stacking of cells is not possible in many high voltage applications due to lack of space. Boost converters can increase the voltage and reduce the number of cells. Two battery-powered applications that use boost converters are [hybrid electric vehicles](http://en.wikipedia.org/wiki/Hybrid_vehicle) (HEV) and lighting systems.

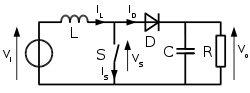
The [Toyota Prius](http://en.wikipedia.org/wiki/Toyota_Prius) HEV uses a 500 V motor. Without a boost converter, the Prius would need nearly 417 cells to power the motor. However, a Prius actually uses only 168 cells and boosts the battery voltage from 202 V to 500 V. Boost converters also power devices at smaller scale applications, such as portable lighting systems. A [white LED](http://en.wikipedia.org/wiki/LED#Ultraviolet.2C_Blue_and_white_LEDs) typically requires 3.3 V to emit light, and a boost converter can step up the voltage from a single 1.5 V alkaline cell to power the lamp. Boost converters can also produce higher voltages to operate [cold cathode](http://en.wikipedia.org/wiki/Cold_cathode) fluorescent tubes (CCFL) in devices such as [LCD](http://en.wikipedia.org/wiki/Liquid_crystal_display) [backlights](http://en.wikipedia.org/wiki/Backlight) and some [flashlights](http://en.wikipedia.org/wiki/Flashlight).



## Circuit analysis

### Operating principle

The key principle that drives the boost converter is the tendency of an inductor to resist changes in current. When being charged it acts as a load and absorbs energy (somewhat like a resistor), when being discharged, it acts as an energy source (somewhat like a battery). The voltage it produces during the discharge phase is related to the rate of change of current, and not to the original charging voltage, thus allowing different input and output voltages.

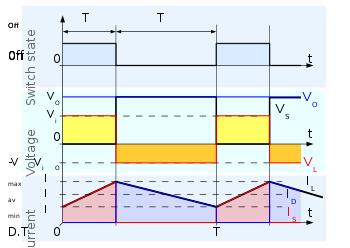
[](http://en.wikipedia.org/wiki/File:Boost_conventions.svg)Boost converter schematic

The two configurations of a boost converter, depending on the state of the switch S.

The basic principle of a Boost converter consists of 2 distinct states (see figure 2):

* In the On-state, the switch S (see figure 1) is closed, resulting in an increase in the inductor current;
* In the Off-state, the switch is open and the only path offered to inductor current is through the [flyback diode](http://en.wikipedia.org/wiki/Flyback_diode) D, the capacitor C and the load R. This results in transferring the energy accumulated during the On-state into the capacitor.
* The input current is the same as the inductor current as can be seen in figure 2. So it is not discontinuous as in the [buck converter](http://en.wikipedia.org/wiki/Buck_converter) and the requirements on the input filter are relaxed compared to a [buck converter](http://en.wikipedia.org/wiki/Buck_converter).

Continuous mode

[](http://en.wikipedia.org/wiki/File:Boost_chronogram.svg)

Waveforms of current and voltage in a boost converter operating in continuous mode.

When a boost converter operates in continuous mode, the current through the inductor (IL) never falls to zero. Figure 3 shows the typical waveforms of currents and voltages in a converter operating in this mode. The output voltage can be calculated as follows, in the case of an ideal converter (i.e. using components with an ideal behaviour) operating in steady conditions:

During the On-state, the switch S is closed, which makes the input voltage (Vi) appear across the inductor, which causes a change in current (IL) flowing through the inductor during a time period (t) by the formula:

\frac{\Delta I_L}{\Delta t}=\frac{V_i}{L}

At the end of the On-state, the increase of IL is therefore:

\Delta I_{L_{On}}=\frac{1}{L}\int_0^{D T}V_i d t=\frac{D T}{L} V_i

D is the duty cycle. It represents the fraction of the commutation period T during which the switch is On. Therefore D ranges between 0 (S is never on) and 1 (S is always on).

During the Off-state, the switch S is open, so the inductor current flows through the load. If we consider zero voltage drop in the diode, and a capacitor large enough for its voltage to remain constant, the evolution of IL is:

V_i-V_o=L\frac{dI_L}{dt}  
Therefore, the variation of IL during the Off-period is:

\Delta I_{L_{Off}}=\int_0^{\left(1-D\right) T}\frac{\left(V_i-V_o\right) dt}{L}=\frac{\left(V_i-V_o\right) \left(1-D\right) T}{L}As we consider that the converter operates in steady-state conditions, the amount of energy stored in each of its components has to be the same at the beginning and at the end of a commutation cycle. In particular, the energy stored in the inductor is given by:

E=\frac{1}{2} L I_L^2

So, the inductor current has to be the same at the start and end of the commutation cycle. This means the overall change in the current (the sum of the changes) is zero:

This can be written as:

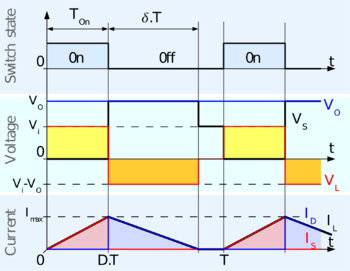
\frac{V_o}{V_i}=\frac{1}{1-D}

Which in turns reveals the duty cycle to be:

D={1-\frac{V_i}{V_o}}

From the above expression it can be seen that the output voltage is always higher than the input voltage (as the duty cycle goes from 0 to 1), and that it increases with D, theoretically to infinity as D approaches 1. This is why this converter is sometimes referred to as a step-up converter.

#### Discontinuous mode

[](http://en.wikipedia.org/wiki/File:Boost_chronogram_discontinuous.png)

Waveforms of current and voltage in a boost converter operating in discontinuous mode.

In some cases, the amount of energy required by the load is small enough to be transferred in a time smaller than the whole commutation period. In this case, the current through the inductor falls to zero during part of the period. The only difference in the principle described above is that the inductor is completely discharged at the end of the commutation cycle (see waveforms in figure 4). Although slight, the difference has a strong effect on the output voltage equation. It can be calculated as follows:

As the inductor current at the beginning of the cycle is zero, its maximum value (at t = DT) is

I_{L_{Max}}=\frac{V_i D T}{L}

During the off-period, IL falls to zero after δT:

I_{L_{Max}}+\frac{\left(V_i-V_o\right) \delta T}{L}=0

Using the two previous equations, δ is:

\delta=\frac{V_i D}{V_o-V_i}

The load current Io is equal to the average diode current (ID). As can be seen on figure 4, the diode current is equal to the inductor current during the off-state. Therefore the output current can be written as:

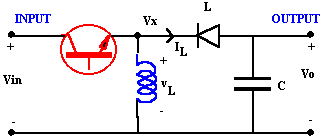
I_o=\bar{I_D}=\frac{I_{L_{max}}}{2}\delta  
Replacing ILmax and δ by their respective expressions yields:

I_o=\frac{V_i D T}{2L}\cdot\frac{V_i D}{V_o-V_i}=\frac{V_i^2 D^2 T}{2L\left(V_o-V_i\right)}Therefore, the output voltage gain can be written as flow:

\frac{V_o}{V_i}=1+\frac{V_i D^2 T}{2L I_o}

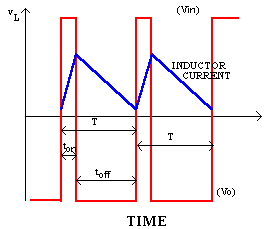
Compared to the expression of the output voltage for the continuous mode, this expression is much more complicated. Furthermore, in discontinuous operation, the output voltage gain not only depends on the duty cycle, but also on the inductor value, the input voltage, the switching frequency, and the output current.

**BUCK-BOOST CONVERTER**



schematic for buck-boost converter

With continuous conduction for the Buck-Boost converter Vx =Vin when the transistor is ON and Vx =Vo when the transistor is OFF. For zero net current change over a period the average voltage across the inductor is zero



Waveforms for buck-boost converter

picture

which gives the voltage ratio

picture

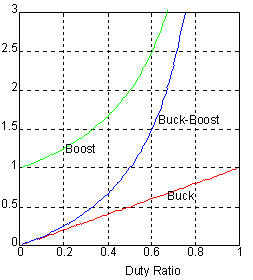
and the corresponding current

picture

Since the duty ratio "D" is between 0 and 1 the output voltage can vary between lower or higher than the input voltage in magnitude. The negative sign indicates a reversal of sense of the output voltage.

## CONVERTER COMPARISON

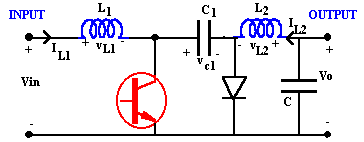
The voltage ratios achievable by the DC-DC converters is summarised in Fig. 10. Notice that only the buck converter shows a linear relationship between the control (duty ratio) and output voltage. The buck-boost can reduce or increase the voltage ratio with unit gain for a duty ratio of 50%.



Comparison of Voltage ratio

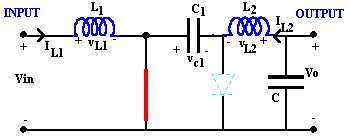
## CUK CONVERTER

The buck, boost and buck-boost converters all transferred energy between input and output using the inductor, analysis is based of voltage balance across the inductor. The CUK converter uses capacitive energy transfer and analysis is based on current balance of the capacitor. The circuit in Fig. 11 is derived from DUALITY principle on the buck-boost converter.



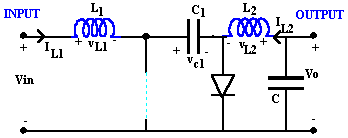
**CUK Converter**

If we assume that the current through the inductors is essentially ripple free we can examine the charge balance for the capacitor C1. For the transistor ON the circuit becomes



CUK "ON-STATE"

and the current in C1 is IL1. When the transistor is OFF, the diode conducts and the current in C1 becomes IL2.



CUK "OFF-STATE"

Since the steady state assumes no net capacitor voltage rise ,the net current is zero

picture

which implies

picture

The inductor currents match the input and output currents, thus using the power conservation rule

picture

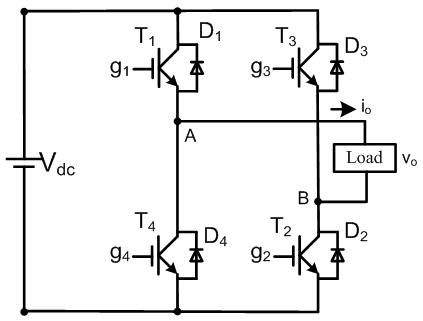
Thus the voltage ratio is the same as the buck-boost converter. The advantage of the CUK converter isthat the input and output inductors create a smooth current at both sides of the converter.

**Voltage Source Inverters (VSI)**

* VSI is fed from a DC voltage source having small or negligible impedance.
* Input voltage is maintained constant.
* Output voltage does not dependent on the load.
* The waveform of the load current as well as its magnitude

depends upon the nature of load impedance.

* VSI requires feedback diodes.

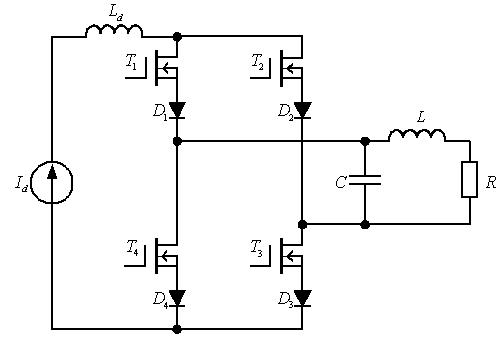


§ The commutation circuit is complicated.

§ Power BJT, Power MOSFET, IGBT and GTO with self-commutation can be used in the circuit.

*Figure 2-2: Current source inverter*

**Current Source Inverters**



* CSI is fed with adjustable current from a DC voltage

source of high impedance.

* The input current is constant but adjustable.
* The amplitude of output current is independent of the

load.

* The magnitude of output

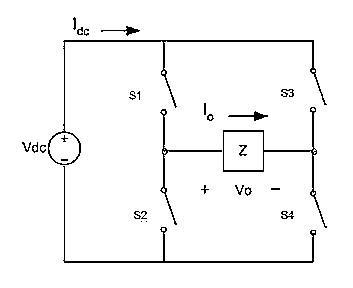
voltage and its waveform

depends upon the nature of the load impedance.

* The CSI does not require any feedback diodes.
* Commutation circuit is simple as it contains only capacitors.

H-Bridge Inverters

As previously mentioned, the purpose of an inverter is to convert DC power to AC power. Inverters are an integral part of many technologies including uninterruptable power supplies, induction heating, high-voltage direct current power transmission, variable frequency drives, electric vehicle drives, and multiple renewable energy applications. All of these technologies use inverters to achieve different goals, but all produce AC power from a DC input. There are many varieties of inverter designs.



**Current source converter**

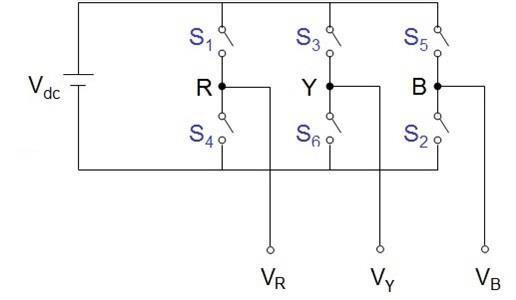
Using the nomenclature above, the switches S1 and S2 should never be closed at the same time, as this would cause a short circuit on the input voltage source. The same applies to the switches S3 and S4. This condition is known as shoot-through.

Its basic configuration is shown in figure. This topology is used in conjunction with either the square wave, or pulse width modulation (PWM) switching schemes.

The square-wave switching scheme is a method for controlling the switches (labelled S1 through S4) in order to achieve a square wave AC output signal. The AC output is achieved by using a control signal with a 50% duty cycle wired to S1 and S4. An inverted copy of the same signal is also wired to S2 and

S3. This switching scheme ensures that S1 and S4 are always on when S2 and S3

Three phase inverter



Basic three phase inverter consist of three legs, each attached to the phase output line. The upper and lower switching transistor are S1 & S4 for R phase, S3 & S6 for Y phase and S5 & S2 for B phase respectively.

**Inverter Applications**

**DC power source utilization**

An inverter converts the DC electricity from sources such as batteries or fuel cells to AC electricity.

**Uninterrupted powers source utilization**

An uninterruptible power supply (UPS) uses batteries and an inverter to supply AC power when main power is not available. When main power is restored, a rectifier supplies DC power to recharge the batteries.

**Electric motor speed control**

Inverter circuits designed to produce a variable output voltage range are often used within motor speed controllers. The DC power for the inverter section can be derived from a normal AC wall outlet or some other source. Control and feedback circuitry is used to adjust the final output of the inverter section which will ultimately determine the speed of the motor operating under its mechanical load.

**Power grid**

Grid-tied inverters are designed to feed into the electric power distribution system. They transfer synchronously with the line and have as little harmonic content as possible. They also need a means of detecting the presence of utility power for safety reasons, so as not to continue to dangerously feed power to the grid during a power outage.

A solar inverter is a balance of system (BOS) component of a photovoltaic system and can be used for both, grid-connected and off-grid systems.

|  |  |  |  |
| --- | --- | --- | --- |
| Solar | inverters | have special functions adapted for | use |
| with | photovoltaic | arrays, including maximum power | point |
| tracking and anti-islanding protection. | | |  |

**HVDC**

With HVDC power transmission, AC power is rectified and high voltage DC power is transmitted to another location. At the receiving location, an inverter in a static inverter plant converts the power back to AC. The inverter must be synchronized with grid frequency and phase and minimize harmonic generation.

Pulse Width Modulation Schemes

**Control techniques for inverter output**

This section examines various methods of output voltage control by means

of inverter gain control. The inverter gain is defined as the ratio of output ac

voltage to input dc voltage. Such gain control is useful in many applications

where the variations of ac output voltage cannot be tolerated due to the

variations in dc input voltage. It is also necessary when volts/Hertz control of

induction motor speeds has to be implemented. The control of motor voltage required along with frequency in order to avoid saturation of the motor magnetic

circuit. Various techniques are available for varying the inverter gain. The most efficient method of controlling the gain and therefore the output voltage to

incorporate Pulse Width Modulation (PWM) control within the inverters. In

addition to PWM method, there are methods involving external control of ac output voltage and dc input voltage. To distinguish these methods from the PWM method, PWM method is referred to as the internal control method the output voltage control is realized by means of modifications in the conduction patterns of the inverter switches. Various methods for the control of output voltage of inverters can be enumerated as follows:

(1) External control of the AC output voltage

(2) External control of the DC input voltage

(3) Internal control of the inverter output voltage

In the first two methods, extra circuits for the control of either dc input

or ac output become necessary. The third method, however, does not require

such circuits. This can be clearly understood in the remaining section that

discusses these methods in considerable detail.

The first two methods require the use of peripheral components

whereas the third method requires no external components. Mostly the

internal control of the inverters is dealt, and so the third method of control discussed in great detail in the following section.

**Internal Pulse Control in inverter**

Inverter output voltage can also be adjusted by exercising a control within

the inverter itself. Pulse width modulation is the most commonly used technique

to control the output voltage of inverter, the various techniques are:

o Single PWM

o Multiple PWM

o Sine PWM

o Space Vector PWM

**Pulse Width Modulation**

Pulse-width modulation (PWM) is the basis for control in power

electronics. The theoretically zero rise and fall time of an ideal PWM waveform represents a preferred way of driving modern semiconductor power devices.

With the exception of some resonant converters, the vast majority of power

electronic circuits are controlled by PWM signals of various forms. The rapid

rising and falling edges ensure that the semiconductor power devices are turned

on or turned off as fast as practically possible to minimize the switching

transition time and the associated switching losses. Although other

considerations, such as parasitic ringing and electromagnetic interference (EMI)

emission, may impose an upper limit on the turn-on and turn-off speed in

practical situations, the resulting finite rise and fall time can be ignored in the

analysis of PWM signals and processes in most cases.

**PWM Duty cycle comparison of inverter**

This is most popular method of controlling the output voltthis method is termed as pulse width modulation technique. PWM is an internal

control method and it gives better result than an external control methods

There are number of PWM methods for variable frequency voltage-sourced

inverters. A suitable PWM technique is employed in order to obtain the require In this method, a fixed dc input voltage is given to the inverter and a controlledac output voltage is obtained by adjusting the on and off periods of the inverter components. Inverters employing PWM principle are called PWM techniques are characterized by constant amplitude pulses. The width these pulses is modulated to obtain inverter output voltage control and to

reduce its harmonic content. **The advantages possessed by PWM**

**technique are**

1. The output voltage control with this method can be obtained without

any additional components.

2. With this method, lower order harmonics can be eliminated or minimized

along with its output voltage control. As higher order harmonics can be

filtered easily, the filtering requirements are minimized.

The main disadvantage of this method is that the SCRs are expensive as they

must possess low turn on and turn off times. This is the most popular method of controlling the output voltage of an inverter in industrial applications. Benefits include – Microprocessor control – Efficient use of power Tolerance to analogy noise – Not susceptible to component drift.

**Multiple PWM**

The harmonic content can be reduced by using several pulses in each

half-cycle of output voltage. The generation of gating signals for turning on

and off transistors is shown in Fig. The gating signals are produced by

comparing reference signal with triangular carrier wave. The frequency of the

reference signal sets the output frequency ( O ) and carrier frequency ( C )

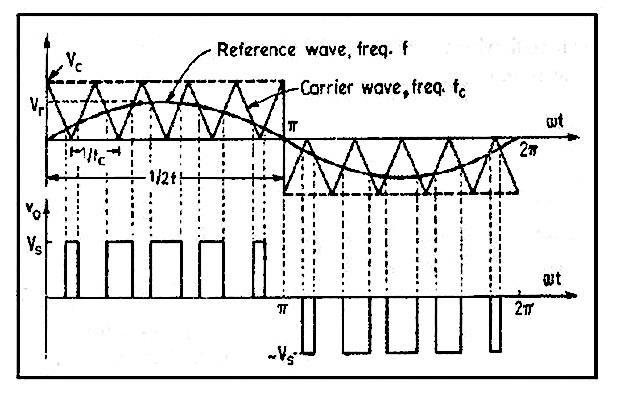
determine the number of pulses per half cycle.

Sine PWM

Sine PWM In single-pulse and multiple pulse modulation techniques the width of all

pulses are same but in sinusoidal pulse width modulation the width of each pulse is varied in proportion to the amplitude of a sine wave. In this technique the gating signals are generated by comparing a sinusoidal reference signal with a triangular carrier wave.

Sine PWM



Comparison and advantage of Multilevel Inverters

*Comparison between Conventional Inverters*

*And Multilevel Inverters*

|  |  |  |
| --- | --- | --- |
| **Sr.no** | **Conventional inverter** | **Multilevel inverter** |
|  |  |  |
| 1 | Higher THD in output voltage | Low THD in output voltage |
|  |  |  |
| 2 | More switching stresses on | Reduced switching stresses on |
|  | devices | devices |
| 3 | Not applicable for high voltage | Applicable for high voltage |
|  | applications | applications |
| 4 | Higher voltage levels are not | Higher voltage levels are produced |
|  | produced |  |
| 5 | Since ⁄ is high, the EMI | Since ⁄ is low, the EMI from the |
|  |  |  |
|  | from the system is high | system is low |
| 6 | Higher switching frequency is | Lower switching frequency can be |
|  | used hence switching losses is | used and hence reduction in |
|  | high | switching losses |
| 7 | Power bus structure, control | Control scheme is complex as the |
|  | schemes are simple | number of levels increases |

**Common Mode Voltage:**

The multilevel inverters produce common mode voltage, reducing the stress of the motor and don’t damage the motor.

**Switching Frequency:**

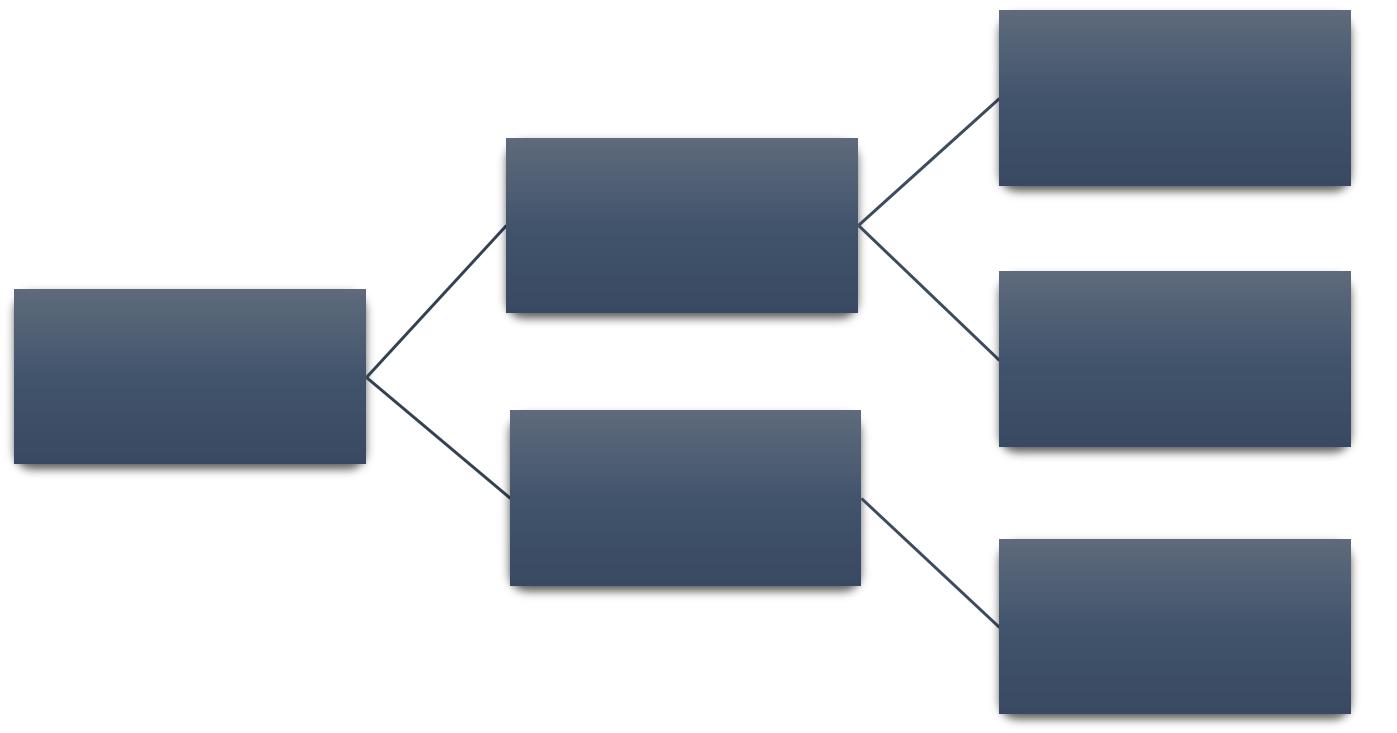
The multilevel inverter can operate at both fundamental switching frequencies

|  |  |  |  |
| --- | --- | --- | --- |
| that are | higher switching | frequency and lower switching | frequency. It |
| should be noted that the | | lower switching frequency | means lower |
| switching loss and higher efficiency is achieved. | | |  |

**Reduced harmonic distortion:**

Selective harmonic elimination technique along with the multi-level topology results the total harmonic distortion becomes low in the output waveform without using any filter circuit.

Types of Multilevel Inverters



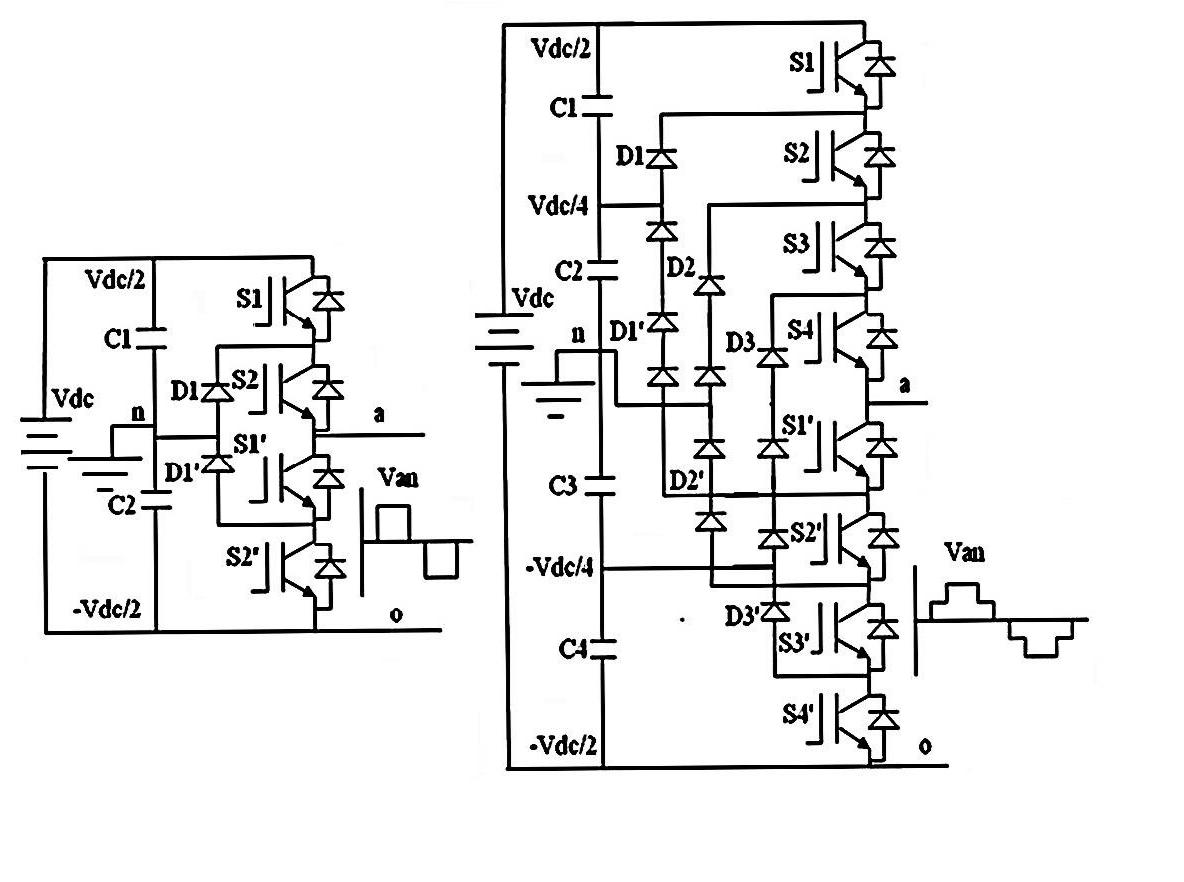
|  |  |
| --- | --- |
|  | Diode clamped |
|  | Inverters |
|  | Common DC |
|  | Sources |
| Multilevel | Flying Capacitor |
| Inverters |
| Inverters |
|  |
|  | Separate DC |
|  | Sources |
|  | Cascaded |
|  | Inverters |
|  | *Types of Multilevel Inverter* |

Multilevel inverters are classified on the basis of the circuit structure and are of three types

**Diode-clamped Multilevel Inverter**

The main concept of this inverter is to use diodes and provides the multiple voltage levels through the different phases to the capacitor banks which are in series. A diode transfers a limited amount of voltage, thereby reducing the stress on other electrical devices. The maximum output voltage is half of the input DC voltage. It is the main drawback of the diode clamped multilevel inverter. This problem can be solved by increasing the switches, diodes, capacitors.

ue to the capacitor balancing issues, these are limited to the three levels. This type of inverters provides the high efficiency because the fundamental frequency used for all the switching devices and it is a simple method of the back to back power transfer systems.



*Topology of the diode-clamped inverter (a) three-level inverter,*

*(b) Five -level inverter*

*Switching sequence for 5 level Diode Clamped Inverter*

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Output** | S1 | S2 | S3 | S4 | S1’ | S2’ | S3’ | S4’ |
|  |  |  |  |  |  |  |  |  |
| VDC | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
|  |  |  |  |  |  |  |  |  |
| VDC/2 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
|  |  |  |  |  |  |  |  |  |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
|  |  |  |  |  |  |  |  |  |
| -VDC/2 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
|  |  |  |  |  |  |  |  |  |
| -VDC | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |

Applications of Diode Clamped Multilevel Inverter:

Static VAR compensation

Variable speed motor drives

High voltage system interconnections

High voltage DC and AC transmission lines

Advantages

When the number of levels is high enough, harmonic content will be low enough to avoid the need for filters.

Efficiency is high due to all devices which are being switched at the fundamental frequency.

We are able to control the reactive power flow.

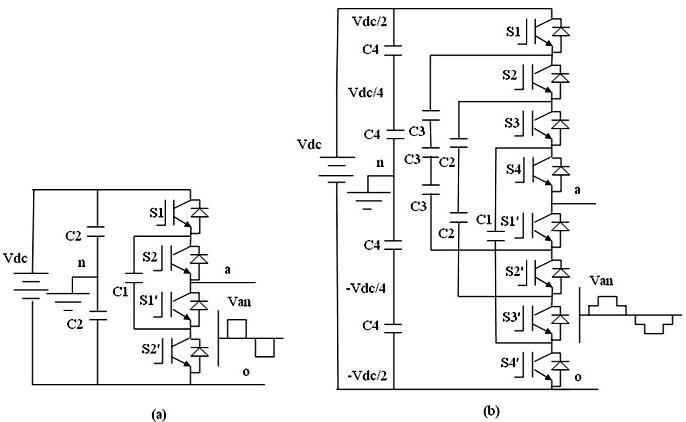
The control method is easy for a back to back intertie system.

Disadvantages

Excessive clamping diodes are being required when the number of levels get high.

It is hard to do a real power flow control for individual converter.

**Flying Capacitor Multilevel Inverter**



***Topology of the Flying Capacitor Multilevel inverter***

***(a) three-level inverter, (b) Five -level inverter***

The main concept of this inverter is to use capacitors. It is of series connection of capacitor clamped switching cells. The capacitors transfer the limited amount of voltage to electrical devices. In this inverter switching states are like in the diode clamped inverter. Clamping diodes are not required in this type of multilevel inverters. The output is half of the input DC voltage. It is drawback of the flying capacitors multi-level inverter. It also has the switching redundancy within phase to balance the flaying capacitors. It can control both the active and reactive power flow. But due to the high frequency switching, switching losses will takes place.

**Applications of Flying Capacitors Multilevel Inverter:**

Induction motor control using DTC (Direct Torque Control) circuit.

Static VAR generation.

Both AC-DC and DC-AC conversion applications.

Converters with Harmonic distortion capability.

Sinusoidal current rectifiers.

**Advantages:**

Huge amount of storage capacitors will provide additional ride through capabilities during power rage.

Switch combination redundancy are provided for balancing different voltage levels.When the number of levels is high enough, the harmonic content will be low enough not to use the filter.We are able to control both the real and reactive power flow, and making a possible voltage source converter candidate for high voltage dc transmission.

Disadvantages:

When the number of converter levels get high, a huge amount of storage capacitor is required. Those high level systems are more difficult to package and those bulky capacitors are expensive.

The switching frequency and switching losses will soar high for real power transmission and the converter control will get very complicated.

***Table 4-3:*** *Switching sequence for 5 level Inverter*

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Output** | S1 | S2 | S3 | S4 | S1’ | S2’ | S3’ | S4’ |
|  |  |  |  |  |  |  |  |  |
| VDC | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
|  |  |  |  |  |  |  |  |  |
| 3VDC/4 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
|  |  |  |  |  |  |  |  |  |
| VDC/2 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
|  |  |  |  |  |  |  |  |  |
| VDC/4 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
|  |  |  |  |  |  |  |  |  |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
|  |  |  |  |  |  |  |  |  |

1. Cascaded Multilevel Inverter

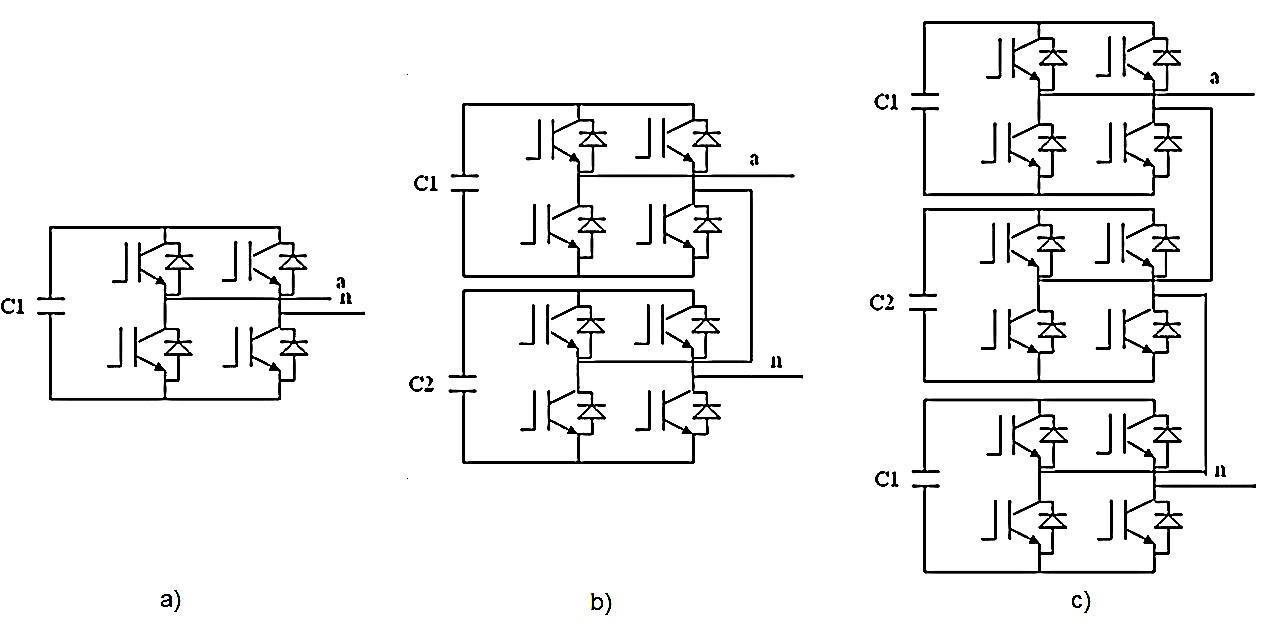
A cascade multilevel inverter is a power electronic device built to synthesize a desired AC voltage from several levels of DC voltages. Such inverters have been the subject of research in the last several years, where the DC levels were considered to be identical in that all of them were either batteries, solar cells, etc. A multilevel converter was presented in which the two separate DC sources were the secondary of two transformers coupled to the utility AC power. In contrast, in this paper, only one source is used without the use of transformers. The interest here is interfacing a single DC power source with a cascade

46

multilevel inverter here the other DC sources are capacitors. Currently, each

phase of a cascade multilevel inverter requires ‘n’ DC sources for 2n+1 levels in

applications that involve real power transfer.



*Figure 4-5: a) Inverter Single Stage b) 5 level Cascaded Inverter c) 7 level Cascaded Inverter*

Applications of Cascaded Multilevel Inverter:

Motor drives Active filters

Electric vehicle drives

DC power source utilization Power factor compensators

Back to back frequency link systems

Interfacing with renewable energy resources.

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Advantages:

The modularized structure allows easy packaging and storage.

The quantity of possible voltage levels is more than DC and FC type.

Disadvantages:

Separated DC sources or capacitor are required for each module.

A more complex controller is required due to the amount of capacitors, which need to be balanced.

1. Comparison of Multilevel Topologies

***Table 4-4:*** *Comparison of multilevel inverter Topologies*

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Sr. |  |  | Topology |  |  | Diode |  |  | Flying |  |  | Cascaded |  |
|  | No. |  |  |  |  | Clamped |  |  | Capacitor |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | Power |  |  |  |  |  |  |  |  |  |  |
|  | 1 |  |  | semiconductor |  |  | 2(m-1) |  |  | 2(m-1) |  |  | 2(m-1) |  |
|  |  |  |  | Switches |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | Clamping | |  |  |  |  |  |  |  |  |  |
| 2 | |  |  | diodes per | |  | (m-1)(m-2) | | 0 | |  | 0 | |  |
|  |  |  |  | Phase | |  |  |  |  |  |  |  |  |  |
|  | 3 |  |  | DC bus |  |  | (m-1) |  |  | (m-1) |  |  | (m-1)/2 |  |
|  |  |  | Capacitors |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | Balancing | |  |  |  |  | (m-1)(m- | |  |  |  |
| 4 | |  |  | capacitors per | | 0 | |  |  | 0 | |  |
|  |  |  | 2)/2 | |  |  |
|  |  |  |  | Phase | |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 5 |  |  | Voltage |  |  | Average |  |  | High |  |  | very small |  |
|  |  |  | unbalancing |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  | Motor drive | |  | Motor drive | |  | Motor drive system, | |
| 6 | |  |  | Applications | |  | system, | |  | system, | |  | PV, fuel cells, | |
|  |  |  |  |  |  |  | STATCOM | |  | STATCOM | |  | battery system | |

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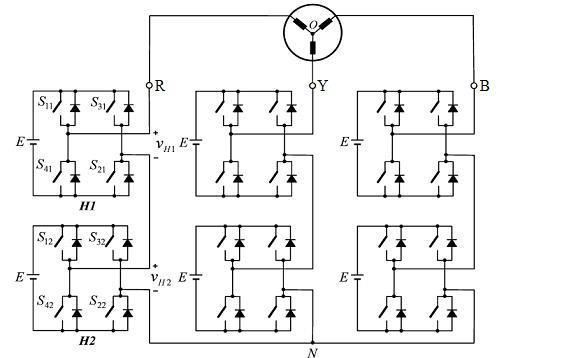
The diode clamped inverters particularly the three-level structure have a wide popularity in motor drive applications besides other multilevel inverter topologies. However, it would be a limitation of complexity and number of clamping diodes for the DCMLIs, as the level exceeds. The FCMLIs are based on balancing capacitors on phase buses and generate multilevel output voltage waveform clamped by capacitors instead of diodes. The FCMLI topology also requires balancing capacitors per phase at a number of (m-1)\*(m-2)/2 for an m-level inverter and it will cause to increase the number of required capacitor in high level inverter topologies and complexity of considering DC-link balancing. Nowadays, the multilevel inverters have become more attractive for researchers and manufacturers due to their advantages over conventional three-level pulse width-modulated (PWM) inverters.

They offer improved output waveforms, smaller filter size, low EMI, lower total harmonic distortion (THD). Multilevel inverter topology has the least components for a given number of levels. Cascaded H-Bridge-MLI topology is based on the series connection of H-bridges with separate DC sources. Since the output terminals of the H-bridges are connected in series, the DC sources must be isolated from each other. The need of several sources on the DC side of the inverter makes multilevel technology attractive for photovoltaic applications.

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4.3 Cascaded Multilevel Inverter

1. Cascaded H-Bridge Inverter with Equal DC voltage



*Figure 4-6: Cascaded H-Bridge with equal DC Voltage*

As the name suggests, the cascaded H-bridge multilevel inverter uses multiple units of H-bridge power cells connected in a series chain to produce high ac voltages. A typical configuration of a five-level CHB inverter is shown in Fig. below, where each phase leg consists of two H-bridge cells powered by two isolated dc supplies of equal voltage E. The CHB inverter in Fig can produce a phase voltage with five voltage levels. When switches S11, S21, S12, and S22 conduct, the output voltage of the H- bridge cells H1 and H2 is VH1 = VH2 = E, and the resultant inverter phase voltage is VAN = VH1 + VH2 = 2E, which is the voltage at the inverter terminal A with respect to the inverter neutral N. Similarly, with S31, S41, S32, and S42 switched on, VAN = –2E. The other three voltage levels are E, 0, and –E, which correspond to various switching states

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summarized in Table. It is worth noting that the inverter phase volt- age VAN may not necessarily equal the load phase voltage VAO, which is the voltage at node A with respect to the load neutral O.

It can be observed from Table that some voltage levels can be obtained by more than one switching state. The voltage level E, for instance, can be produced by four sets of different (redundant) switching states. The switching state redundancy is a common phenomenon in multilevel converters. It provides a great flexibility for switching pattern design, especially for space vector modulation schemes.

Switching table for 5 level CHB inverter:

***Table 4-5:*** *Switching table for 5 level*

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Output** |  |  |  |  |  | **Switching State** | | | | |  |  |  |  | **VH1** |  |  | **VH1** |  |
|  | **Voltage** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | S11 |  |  | S31 |  |  | S12 |  |  | S32 |  |  |  |  |  |
|  | **VAN** |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | **2E** | | 1 | |  | 0 | |  | 1 | |  | 0 | |  |  | E | |  | E | |
|  |  |  |  | 1 |  |  | 0 |  |  | 1 |  |  | 1 |  |  | E |  |  | 0 |  |
|  | **E** |  | 1 | |  | 0 | |  | 0 | |  | 0 | |  |  | E | | 0 | |  |
|  |  |  | 1 |  |  | 1 |  |  | 1 |  |  | 0 |  |  | 0 |  |  | E |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | 0 | |  | 0 | |  | 1 | |  | 0 | |  | 0 | |  |  | E | |
|  |  |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |
|  |  |  | 0 | |  | 0 | |  | 1 | |  | 1 | |  | 0 | |  | 0 | |  |
| **0** | |  |  | 1 |  |  | 1 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |
|  | 1 | |  | 1 | |  | 1 | |  | 1 | |  | 0 | |  | 0 | |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  | 1 |  |  | 0 |  |  | 0 |  |  | 1 |  |  | E |  |  | -E |  |
|  |  |  | 0 | |  | 1 | |  | 1 | |  | 0 | |  |  | -E | |  | E | |
|  |  |  |  | 0 |  |  | 1 |  |  | 1 |  |  | 1 |  |  | -E |  |  | 0 |  |
|  | **-E** |  | 0 | |  | 1 | |  | 0 | |  | 0 | |  |  | -E | | 0 | |  |
|  |  |  | 1 |  |  | 1 |  |  | 0 |  |  | 1 |  |  | 0 |  |  | -E |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | 0 | |  | 0 | |  | 0 | |  | 1 | |  | 0 | |  |  | -E | |
|  | **-2E** | |  | 0 |  |  | 1 |  |  | 0 |  |  | 1 |  |  | -E |  |  | -E |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

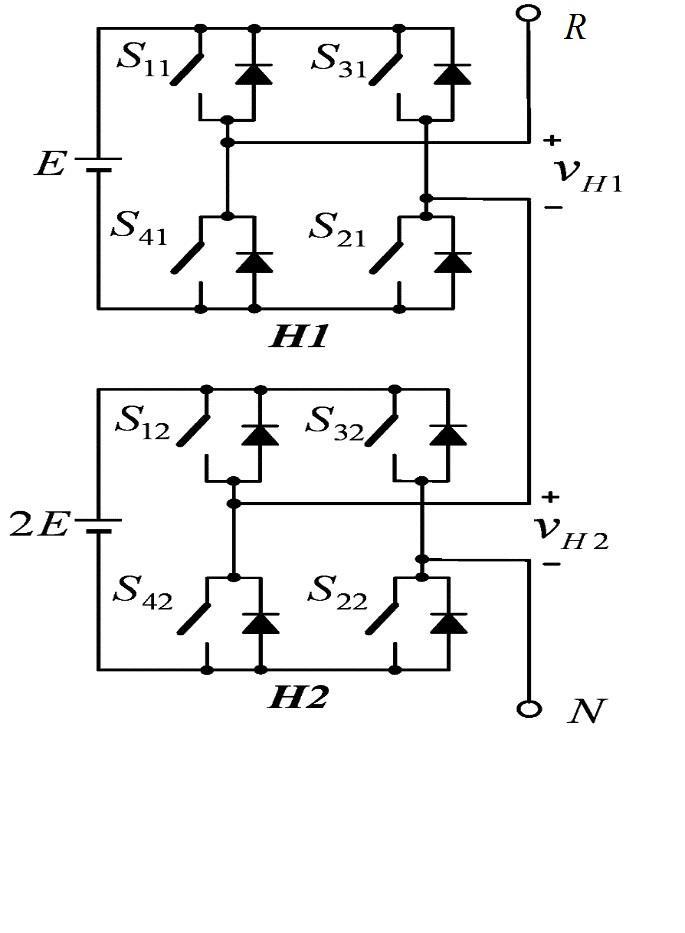
*Equal DC CHB inverter*

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*Figure 4-7: One leg with unequal DC voltage*

1. Cascaded H-Bridge Inverter with Unequal DC voltage

To operate a seven level cascaded multilevel converter consider two unequal dc sources, the magnitude of voltage of first dc source is E and the second DC source is 2E. With unequal DC voltages, the number of voltage levels can be increased without necessarily increasing the number of H-bridge cells in cascade. This allows more voltage steps in the inverter output voltage waveform for a given number of power cells. Figure 4-7 shows two inverter topologies,



where the dc voltages for the H- bridge cells are not equal. In the seven-level topology, the dc voltages for H1H2 are E and 2E, respectively. The two-cell inverter leg is able to produce seven voltage levels: 3E, 2E, E, 0, –E, –2E, and

–3E. The relationship between the voltage levels and their corresponding switching states is summarized in Table. In the nine-level topology, the dc voltage of H2 is three times that of H1. All the nine voltage levels can be obtained by replacing the H2 output voltage of VH2 = ±2E in Table with VH2 = ±3E and then calculating the inverter phase voltage VAN.

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Switching table for 7 level CHB inverter:

***Table 4-6****: Switching table for 7 level unequal DC CHB inverter*

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Output** |  |  | **Switching State** | |  | **VH1** | **VH1** |
|  | **Voltage** |  | S11 | S31 | S12 | S32 |  |  |
|  | **VAN** |  |  |  |
|  |  |  |  |  |  |  |  |
|  | **3E** | | 1 | 0 | 1 | 0 | E | 2E |
|  | **2E** | | 1 | 1 | 1 | 0 | 0 | 2E |
|  |  |  | 0 | 0 | 1 | 0 | 0 | 2E |
|  | **E** |  | 1 | 0 | 1 | 1 | E | 0 |
|  |  |  | 1 | 0 | 0 | 0 | E | 0 |
|  |  |  | 0 | 1 | 1 | 0 | -E | 2E |
| **0** | |  | 0 | 0 | 0 | 0 | 0 | 0 |
|  |  |  | 0 | 0 | 1 | 1 | 0 | 0 |
|  |  |  | 1 | 1 | 0 | 0 | 0 | 0 |
|  |  |  | 1 | 1 | 1 | 1 | 0 | 0 |
|  | **-E** | | 1 | 0 | 0 | 1 | E | -2E |
|  |  |  | 0 | 1 | 1 | 1 | -E | 0 |
|  |  |  | 0 | 1 | 0 | 0 | -E | 0 |
|  | **-2E** |  | 1 | 1 | 0 | 1 | 0 | -2E |
|  |  |  | 0 | 0 | 0 | 1 | 0 | -2E |
|  | **-3E** | | 0 | 1 | 0 | 1 | -E | -2E |
|  |  |  |  |  |  |  |  |  |

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5 Multilevel Inverter PWM

schemes

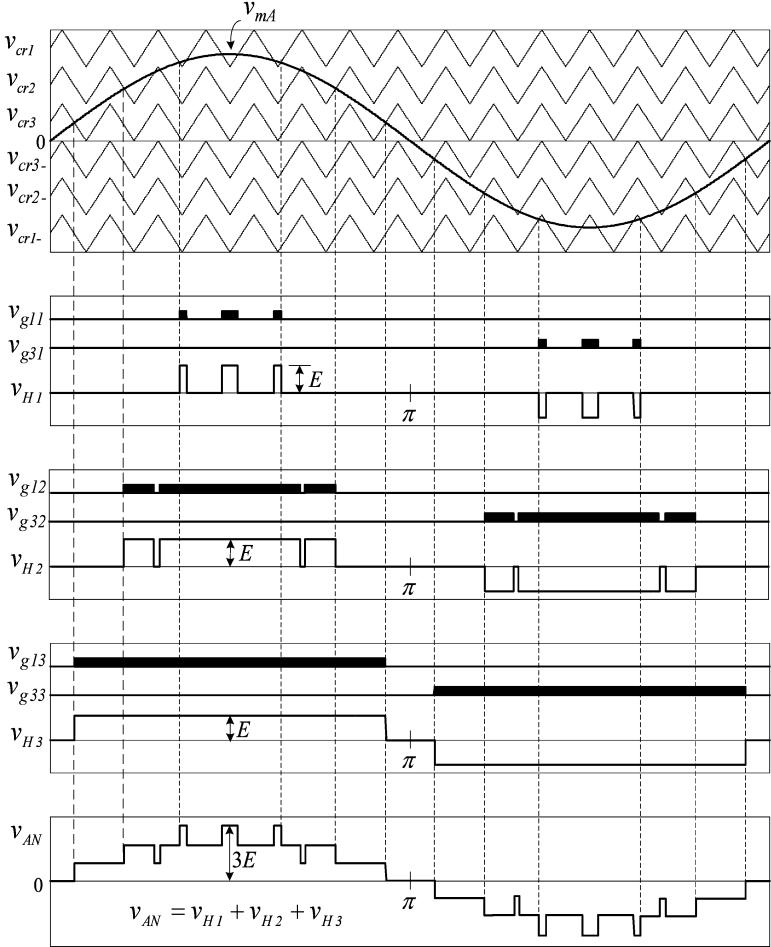
Carrier based PWM schemes:

The carrier-based modulation schemes for multilevel inverters can be

generally classified into two categories: phase-shifted PWM and level-shifted

PWM.

Both modulation schemes can be applied to the CHB inverters.



*Figure 5-1: Level-shifted PWM for a Seven-level CHB inverter*

*(mf = 15, ma = 0.8, fm = 50 Hz and fcr = 900 Hz)*

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5.1 Level Shifted Sine PWM scheme

For carriers signals, the time values of each carrier waves are set to [0 1/600 1/300] while the outputs values are set according to the disposition of carrier waves.

After comparing, the output signals of comparator are transmitted to the IGBT. It requires (m-1) triangular carriers, all having the same frequency and amplitude. The frequency modulation index is given by mf = fcr/fm. The switching frequency of the inverter using the level-shifted modulation is equal to the carrier frequency, that is, (device switching frequency) fC = fcr. Average device switching frequency is device switching frequency) fC = fcr/ (m – 1).The conduction time of the devices is not evenly distributed either.

|  |  |  |  |
| --- | --- | --- | --- |
|  | ̂ | |  |
| = |  |  | 0 ≤ ≤ 1 |
| ̂ | |
|  | ( − 1) | |  |

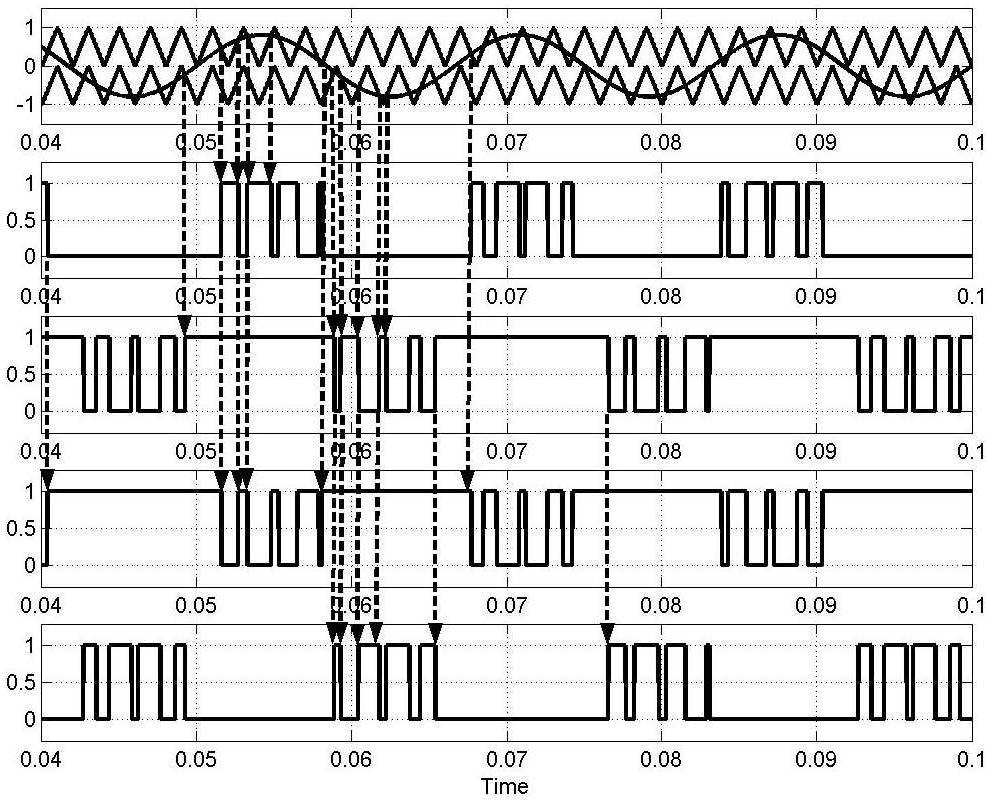
Where, ̂ is the peak amplitude of the modulating wave ̂ and ̂cr is the peak amplitude of each carrier wave.

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5.2 Types of Level Shifted Sine PWM

1. In-Phase Disposition IPD

In-Phase Disposition (IPD), where all carriers are in phase.



*Figure 5-2: Switching pattern produced using the IPD carrier-based PWM scheme:*

*(a) Two triangles and the modulation signal (b) S1RY (c) S2RY (d) S1RN (e) S2RN*

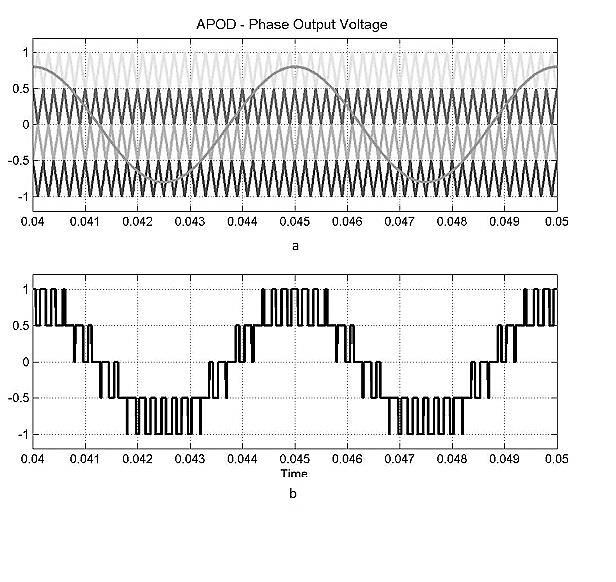
All the carrier signals are in phase.

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1. Alternative Phase opposite Disposition APOD

Alternative Phase Opposite Disposition (APOD), where all carriers are

alternatively in opposite disposition.



*Figure 5-3: Simulation of carrier-based PWM scheme using APOD for a five-level inverter. (a) Modulation signal and carrier waveforms*

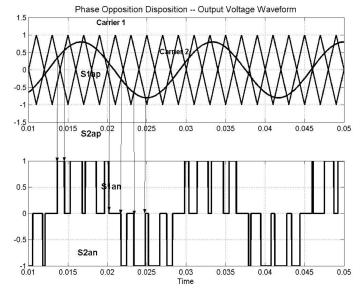
*(b) Phase “R” output voltage*

All the carriers above zero reference are in phase but are in opposition

with those below zero reference.

**Phase Opposite Disposition POD**

Phase Opposite Disposition (POD), where all carriers above the zero reference are in phase but in opposition with those below the zero reference.



*Simulation of carrier-based PWM scheme using POD.*

1. *Modulation signal and phase carrier waveforms*
   1. *Phase “R” output voltage.*

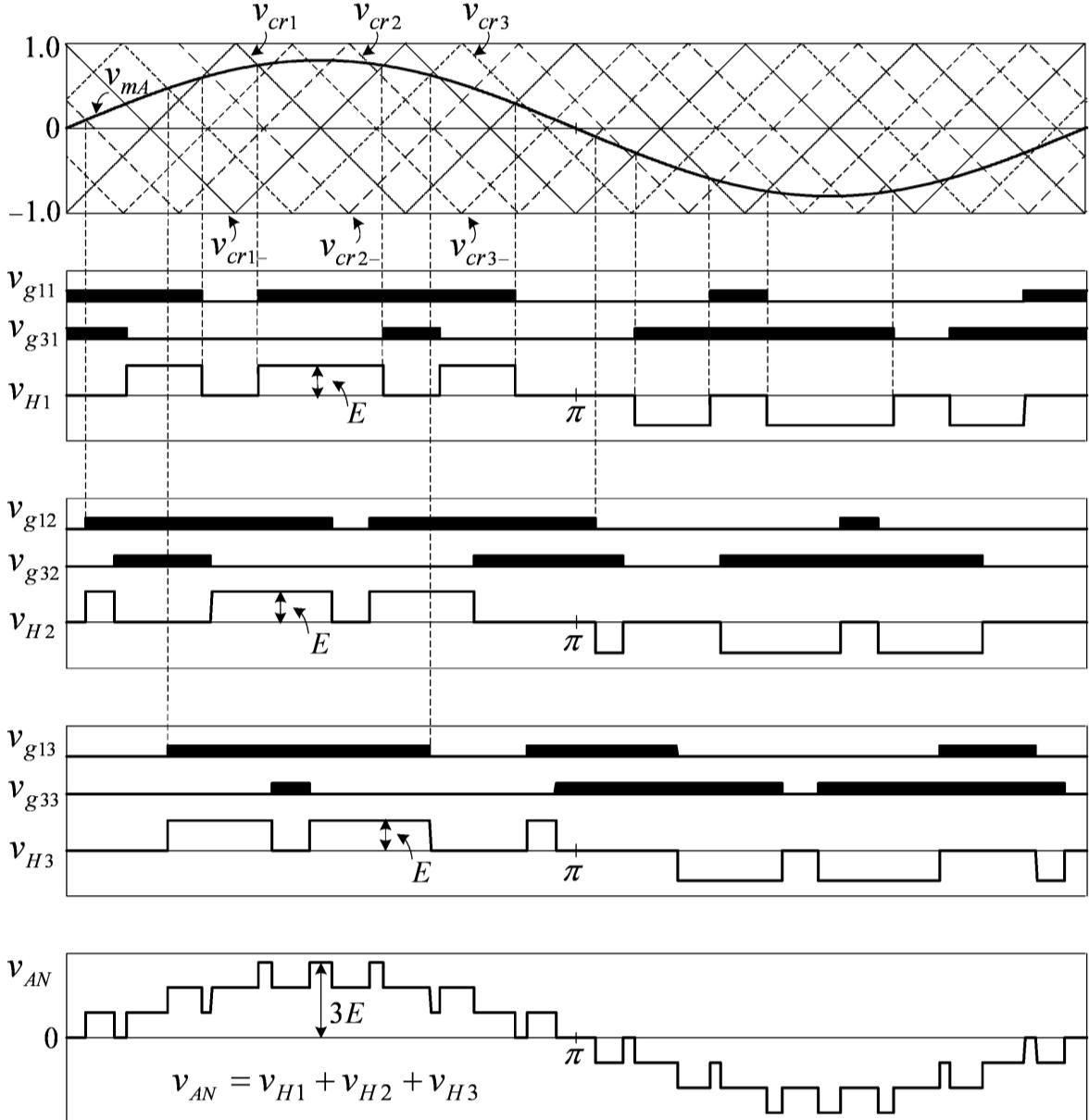
The modulating signal of each phase is displaced from each other by 120°. All the carrier signals have same frequency FC and amplitude AC while the modulating signal has a frequency of fm and amplitude of Am. The fc should be in integer the multiples of fm with three-times. This is required for all the modulating signal of all the three phases see the same carriers, as they are 120° apart. The carrier waves and the modulating signals are compared and the output of the comparator defines the output in the position.

signal is greater than that of the carrier wave and zero otherwise. Similarly for

the negative half cycle, if the modulating signal is lower than the carrier wave

the output of the comparator is high and zero otherwise.

Phase Shifted Sine PWM scheme



In general, a multilevel inverter with m voltage levels requires (m – 1) triangular carriers In the phase-shifted multicarrier modulation, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by PhCR = 360°/(m –

**CONCLUSION**

**In this paper, an improved five-level CMLI with low switch count for the minimization of leakage current in a transformer-less PV system was proposed. The proposed CMLI minimized the leakage current by eliminating the high-frequency transitions in the terminal and CMVs. The proposed topology also reduced conduction and switching losses which made it possible to op-erate the CMLI at high switching frequency. Furthermore, the solution for generalized 2m + 1 levels CMLI was also presented in the paper. The given PWM technique required only one carrierwave for the generation of 2m + 1 levels. The operation, analysis of terminal, and CMVs for the CMLI were also presented in the paper. The simulation and experimental results validated the analysis carried out in this paper. The MPPT algorithm was also integrated with the proposed five-level CMLI to extrac the maximum power from the PV panels.**

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